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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,842	03/03/2004	Shih-Lun Chen	3111-425	2005
75	90 03/31/2006		EXAMINER	
BRUCE H. TROXELL			HERNANDEZ, WILLIAM	
SUITE 1404 5205 LEESBUI	RG PIKE		ART UNIT	PAPER NUMBER
FALLS CHURCH, VA 22041			2816	
			DATE MAILED: 03/31/2000	6

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)				
Office Action Summary		10/790,842	CHEN ET AL.				
		Examiner	Art Unit				
		William Hernandez	2816				
	The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SH WHIC - Exter after - If NC - Failu Any	ORTENED STATUTORY PERIOD FOR REPLICATION OF THE MAILING DONA INSIGN OF THE	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be timwill apply and will expire SIX (6) MONTHS from a cause the application to become ABANDONE	I. lety filed the mailing date of this communication. O (35 U.S.C. § 133).				
Status							
1)[🗆	Responsive to communication(s) filed on <u>03 M</u>	farch 2004.					
·		action is non-final.					
3)	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
	closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Dispositi	on of Claims		·				
4)⊠	4) Claim(s) 1-5 is/are pending in the application.						
	4a) Of the above claim(s) is/are withdrawn from consideration.						
5)[Claim(s) is/are allowed.						
6)⊠	Claim(s) <u>1-5</u> is/are rejected.						
·	Claim(s) is/are objected to.						
8)[8) Claim(s) are subject to restriction and/or election requirement.						
Applicati	on Papers	•					
9)⊠ The specification is objected to by the Examiner.							
10)⊠ The drawing(s) filed on <u>03 March 2004</u> is/are: a) accepted or b)⊠ objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).							
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
Priority u	ınder 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 							
2) D Notic 3) Inform	t(s) e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) r No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal Pa					

DETAILED ACTION

Drawings

1. Figures 1, 2A, 2B, 3 and 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abevance.

Specification

2. The disclosure is objected to because of the following informalities: the word "small" on page 4 line 29 is incorrectly used. Perhaps the applicant meant to say "smaller". Also, on page 5 line 24 the second appearance of the unit for voltage (V) is not preceded by any value. Perhaps the applicant meant to say "0V".

Appropriate correction is required.

3. The claims are objected to because they include reference characters which are not enclosed within parentheses.

Reference characters corresponding to elements recited in the detailed description of the drawings and used in conjunction with the recitation of the same element or group of elements in the claims should be enclosed within parentheses so as to avoid confusion with other numbers or characters which may appear in the claims. See MPEP § 608.01(m).

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Claim Rejections - 35 USC § 112

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4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

- 5. Claims 1 and 2 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
- 6. The terms "low-voltage", "high-voltage" and "low-cost" in claim 1 are relative terms which renders the claim indefinite. The terms "low-voltage", "high-voltage" and "low cost" are not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.
- 7. The term "receivable" is not a positive limitation. It is not clear if the plural MOSFETs are receiving or not receiving.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 8. Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Tailliet (6,549,048).

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Tailliet Fig. 3 shows a main circuit (10, 11), being composed of three P-type (T1, T2, T5) and three N-type (T3, T4, T6) MOSFETs, and the operation thereof being controlled by the voltage over a node A (N2) and a node B (N1); a first protection circuit, being composed of four P-type MOSFETs (T300, T301, T20, T22), for ensuring the voltage at the node A is larger than a specified low voltage value; and a second protection circuit, being composed of four N-type MOSFETs (T310, T311, T21, T23), for ensuring the voltage at the node B is smaller than a specified high voltage value as called for in claim 1.

Regarding claim 2, Taillet Fig. 3 further shows the Schmitt trigger of claim 1, wherein the maximum voltage the plural MOSFETs are capable of receiving is 2.5V.

9. Claims 1-2 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al. (6,870,413B1).

Chang et al. Fig. 4 shows a main circuit, being composed of three P-type (T4, T5, T21) and three N-type (T0, T1, T20) MOSFETs, and the operation thereof being controlled by the voltage over a node A (140) and a node B (150); a first protection circuit, being composed of four P-type MOSFETs (T7, T8, T9, T10), for ensuring the voltage at the node A is larger than a specified low voltage value; and a second protection circuit, being composed of four N-type MOSFETs (T11, T12, T13, T14), for ensuring the voltage at the node B is smaller than a specified high voltage value as called for in claim 1.

Regarding claim 2, Chang et al. Fig. 4 further shows the Schmitt trigger of claim 1, wherein the maximum voltage the plural MOSFETs are capable of receiving is 2.5V.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 11. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (6,870,413B1).

Chang et al.'s figure 4 discloses the invention set forth in claim 1 but does not disclose expressly a low voltage value of 0.8V as called for in claim 3. Chang et al. teaches in col. 4, line 63, that typical threshold voltages of transistors in a Schmitt trigger circuit range from 0.3 to 1.0V. Therefore, it would been obvious to a person of ordinary skill in the art at the time the invention was made to set a voltage threshold of at least 0.4V to Chang et al.'s circuit and maintain a node (Fig. 4, 140) voltage of 0.8V. Therefore, outside of non-obvious results, the obviousness of selecting transistors' threshold voltages to set up the hysteresis level is an obvious modification of Chang et al., thus, will not be patentable under 35USC 103(a).

Regarding claim 4, Chang et al. reference does not disclose expressly a high voltage value of 2.5V. Chang et al. teaches in col. 4, line 63, that typical threshold voltages of transistors in a Schmitt trigger circuit range from 0.3 to 1.0V. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to set a voltage threshold of at least 0.4V to Chang et al.'s circuit and maintain a node (Fig. 4, 150) voltage of 2.5V. Therefore, outside of non-obvious results, the obviousness of selecting transistors' threshold voltages to set

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up the hysteresis level is an obvious modification of Chang et al., thus, will not be patentable under 35USC 103(a).

12. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tailliet (6,549,048B2) in view of Pizzuto et al. (6,147,566).

Tailliet discloses the invention set forth in claim 1 but does not disclose expressly a native MOSFET in the second protection circuit as called for in claim 5. Pizzuto et al. discloses in Fig. 10 a circuit whose N channel MOS type transistors are native transistors so as to limit the losses in these transistors and so as to enable the use of the circuit with a low supply voltage (col. 13, lines 21-25). Therefore, it would been obvious to a person of ordinary skill in the art at the time of the invention to replace Tailliet's N-type MOSFET's (T310, T311, T21, T23) with native MOSFETS for the purpose of lowering power consumption and to increase efficiency.

13. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (6,870,413B1) in view of Pizzuto et al. (6,147,566).

Chang et al. discloses the invention set forth in claim 1 but does not disclose expressly a native MOSFET in the second protection circuit as called for in claim 5. Pizzuto et al. discloses in Fig. 10 a circuit whose N channel MOS type transistors are native transistors so as to limit the losses in these transistors and so as to enable the use of the circuit with a low supply voltage (col. 13, lines 21-25). Therefore, it would been obvious to a person of ordinary skill in the art at the time of the invention to replace Chang et al.'s N-type MOSFET's (T11, T12, T13, T14) with native MOSFETS for the purpose of lowering power consumption and to increase efficiency.

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Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hirose (6,388,487 B1), Hoeld (6,046,617), Shin (5,874,844), and Singh (6,091,265) are cited to teach Schmitt/hysteresis circuits featuring combinations of P-MOS and N-MOS transistors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Hernandez whose telephone number is (571) 272-8979. The examiner can normally be reached on Mon.-Fri. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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TUANT. LAM
PRIMARY EXAMINER